Abstract

The present invention is a converter stage for converting a differential logic input signal and a corresponding common mode differential logic signal each having a first single-ended logic signal and a complementary second single-ended logic signal into a single-ended logic output signal. The converter stage comprises a first and a second differential stage each having a first and a second MOS transistor and a first and second current source for the differential stages. According to the invention the current sources are controlled by the voltage level which is centered between the mid-potentials of the common mode level differential logic signal and the mid-potential of the differential logic input signal.

Figure 4